AMENDMENTS TO THE CLAIMS

1. (Original) A programmable read only memory cell useful in a memory array having select and access lines, the memory cell comprising:

a MOS field effect transistor having a gate, a gate dielectric underlying the gate, and first and second doped semiconductor regions underlying both the gate dielectric and the gate in a spaced apart relationship to define a channel region therebetween;

a MOS data storage element having a conductive structure, an ultra-thin dielectric underlying the conductive structure, and a first doped semiconductor region underlying both the ultra-thin dielectric and the conductive structure, the first doped semiconductor region of the MOS data storage element being coupled to the first doped semiconductor region of the MOS field effect transistor;

a select line segment coupled to the gate of the MOS field effect transistor;

a first access line segment coupled to the second doped semiconductor region of the MOS field effect transistor; and

a second access line segment coupled to the conductive structure of the MOS data storage element.

2. (Original) The memory cell of Claim 1 wherein each of the MOS data storage elements comprises an inversion-enabled region underlying both the ultra-thin dielectric and the conductive structure and adjacent to the first doped region of the MOS data storage element.

3. (Original) The memory cell of Claim 1 wherein each of the MOS data storage elements comprises a second doped region underlying both the ultra-thin dielectric and the conductive structure and integrated with the first doped region of the MOS data storage element.

4. (Original) The memory cell of Claim 1 wherein the gate dielectric of the MOS field effect transistors and the ultra-thin dielectric of the MOS data storage elements are formed from a common layer of ultra-thin gate oxide.

5. (Original) The memory cell of Claim 1 wherein the gate dielectric of the MOS field effect transistors is thicker than the ultra-thin dielectric of the MOS data storage elements.

6. (Cancelled)
7. (Cancelled)
8. (Cancelled)
9. (Cancelled)
10. (Cancelled)
11. (Cancelled)
12. (Cancelled)
13. (Cancelled)
14. (Cancelled)

15. (Original) A programmable read only memory array comprising a plurality of row lines, a plurality of column lines, at least one shared line, and a plurality of memory cells at respective crosspoints of the row lines and column lines in the memory, each of the memory cells comprising:

a MOS field effect transistor having a gate, a gate dielectric underlying the gate, and first and second doped semiconductor regions underlying both the gate dielectric and the gate in a spaced apart relationship to define a channel region therebetween; and

a MOS data storage element having a conductive structure, an ultra-thin dielectric underlying the conductive structure, and a first doped semiconductor region underlying both the ultra-thin dielectric and the conductive structure, the first doped semiconductor region of the MOS data storage element being coupled to the first doped semiconductor region of the MOS field effect transistor;

wherein one of the column lines is coupled to the second doped semiconductor region of the MOS field effect transistor or to the conductive structure of the MOS data storage element, and one of the at least one shared lines is coupled to the conductive structure of the MOS data storage element or to the second doped semiconductor region of the MOS field effect transistor.

16. (Original) The memory array of Claim 15 wherein each of the MOS data storage elements comprises an inversion-enabled region underling both

the ultra-thin dielectric and the conductive structure and adjacent to the first doped region of the MOS data storage element.

17. (Original) The memory array of Claim 15 wherein each of the MOS data storage elements comprises a second doped region underling both the ultra-thin dielectric and the conductive structure and integrated with the first doped region of the MOS data storage element.

18. (Original) The memory array of Claim 15 wherein the gate dielectric of the MOS field effect transistors and the ultra-thin dielectric of the MOS data storage elements are formed from a common layer of ultra-thin gate oxide.

19. (Cancelled)
20. (Cancelled)
21. (Cancelled)
22. (Cancelled)
23. (Cancelled)
24. (Cancelled)
25. (Cancelled)
26. (Cancelled)
27. (Cancelled)
28. (Cancelled)
29. (Cancelled)
30. (Cancelled)
31. (Cancelled)